A New CMOS Current-Mode Folding Amplifier

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Abstract. *In this paper, a new CMOS current-mode folding amplifier is proposed. The circuit is designed using MOSFETs operating in strong inversion. The design produces a nearly ideal saw-tooth input-output characteristic which is a mandatory requirement in folding analog-to-digital converters. The functionality of the proposed circuit was confirmed using Tanner simulation tools in 0.35 μm CMOS technology. Simulation results are in excellent agreement with the theory.*

Keywords

Current-mode, saw-tooth generator, folding amplifier, Flash analog-to-digital converter.

1. Introduction

The analog-to-digital converter (ADC) is one of the most important building blocks to interface analog world to digital world. ADCs applications are widely used in numerous applications including digital telephone transmission, cell phones, medical imaging and wireless nodes.

ADCs are found in different architectures and each one has a unique set of characteristics and different limitations. Consequently, the most convenient analog-to-digital conversion technique should be chosen based on the application. The most common types of ADCs are flash, successive approximation and sigma-delta. The fastest and conceptually simplest conversion process is the full flash or parallel flash ADC [1], [2]. However, for N-bit resolution, it needs a $2^N - 1$ comparators, and 2^N resistors to generate reference voltages, which leads to higher power consumption and larger silicon area.

Folding ADC is used to reduce the complexity of flash ADC while maintaining a relatively good conversion speed. For example, for ($N = m + l$) bits resolution, with m most significant bits and l least significant bits, the number of comparators required for folding ADC is $2^m - 1$ comparators (for MSB) and $2^l - 1$ comparators (for LSB). The total number of comparators used is $(2^m - 1) + (2^l - 1)$ which can be as low as less than half of the number of comparators used in flash ADC which is $2^N - 1$.

On the other hand, the applications of CMOS current-mode circuits have increased dramatically. Current-mode circuits have some recognized advantages over voltage-mode counterparts. The current-mode circuits are more suitable for low voltage design compared to voltage mode circuits.

A key element in the design of the folding ADC is the folding amplifier having a saw-tooth input-output characteristic. A conventional voltage-mode folding amplifier is built around a differential pair [3], [4]. It is well known, however, that the differential pair is not suitable for low voltage design because of nonlinearity problems [5]. Moreover, the input-output characteristic of a differential amplifier-based folding amplifier is sine-wave shaped. This would result in digitization error. A current-mode folding amplifier based on current mirror was proposed in [6]. In reference [7], the authors presented a current-mode folding amplifier controlled by coarse ADCs for the design of a current-mode folding ADC. The input-output characteristic of the amplifiers proposed in [6], [7] is a triangular-wave which will degrade the conversion accuracy. Recently, some pure linear analog preprocessing voltage-mode folding circuits have been presented to generate saw-tooth input-output characteristic [8], [9].However, in the open literature, there are no current-mode folding circuits that generate saw-tooth input-output characteristic.

In this paper, a new CMOS current-mode folding amplifier that generates a saw-tooth input-output characteristic is presented. The paper is organized as follows. Section 2 presents a brief description of the folding concept. The proposed design is presented in Section 3. Simulation results are presented in Section 4. Mismatch analysis study is described in Section 5. The paper conclusion is presented in Section 6.

2. Folding ADC

Folding is a type of analog preprocessing that is used to produce more than one zero-crossing point. Folding is used to reduce the number of comparators, and thus, the power consumption and the silicon area of a flash ADC. The block diagram of a current-mode folding ADC is shown in Fig 1. The input signal is applied to an analog preprocessing circuit called folding amplifier, and the output of this folding circuit is connected to a fine quantizer. Also, the input signal is directly connected to a coarse quantizer. The coarse digital output represents the most significant bits (MSB) and the fine digital output will produce the least significant bits (LSB).

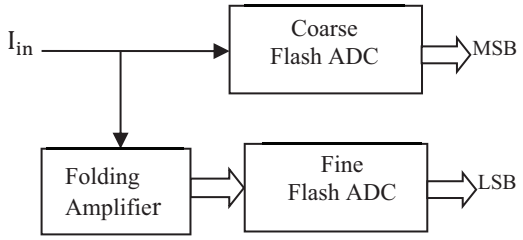


Fig. 1. Block diagram of current-mode folding flash ADC.

The output of the folding amplifier could be saw-tooth, triangular or sinusoidal-shaped based on the architecture. Folding the input to a triangular or sinusoidal-shaped output will lead to errors in the digitized output and compensation would be required. As an example a 5-bits folding ADC and errors produced from triangular-shaped output folding amplifier is shown in Fig 2. It is clear from Fig. 2 that the digital output, 01010, is the same for the two different analog inputs, $0.36I_{FS}$ and $0.46I_{FS}$. Thus, one digital output represents two analog inputs.

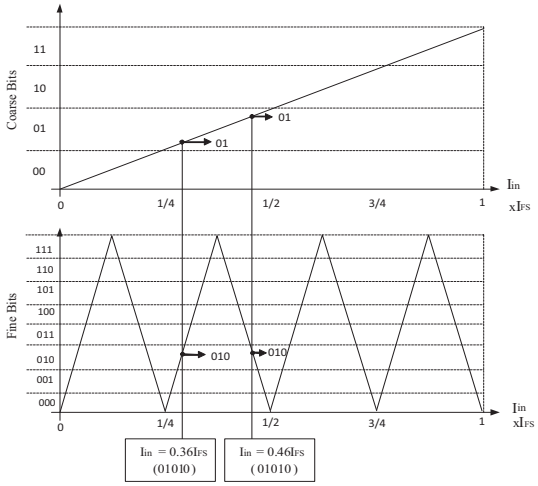


Fig. 2. 5-bit folding ADC using triangular-shaped folding amplifier.

It is well known that saw-tooth input-output characteristic is the best that will eliminate, or minimize, the digitization error as depicted in Fig. 3. Here it is clear that only one digital output represents one analog input.

3. Proposed Current-Mode Folding Amplifier

A current-mode folding amplifier has been developed to generate saw-tooth-shaped input-output characteristic. Fig. 4 shows the concept used to develop the proposed folding amplifier. It consists of two blocks each block produces the shape of the signal shown in Fig. 4 and the two signals are summed together to produce the required saw-tooth input-output characteristic.

A possible realization for block1 of Fig. 4 is shown in Fig. 5(a). It consists of two current mirrors connected in

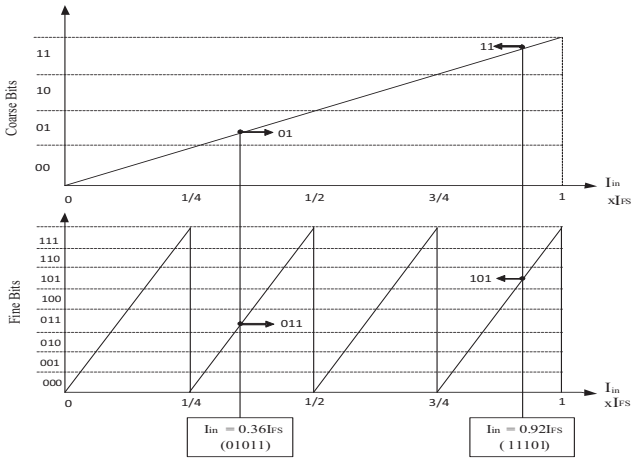


Fig. 3. 5-bit folding ADC using saw-tooth-shaped of folding amplifier.

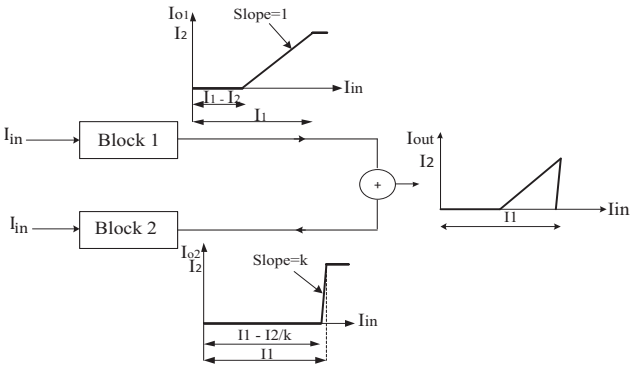


Fig. 4. The concept used in developing the proposed folding amplifier.

cascade. The circuit is designed so that for small input current, the output is zero, while for large input current the output current is constant and equal to αI_2 where I_2 is the bias current and α is the aspect ratio of transistors M1 and M2. The output current as a function of the input current for the block1 is shown in Fig. 5(b).

With reference to Fig. 5(a), the output current is given by:

$$I_{o1} = I_2 \frac{\alpha_4}{\alpha_3} - I_1 \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3} + I_{in} \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3} \tag{1}$$

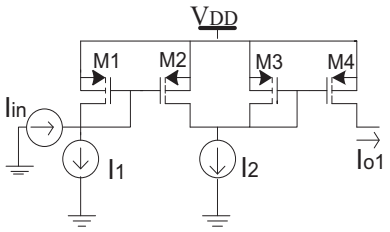
where $a_i = W_i / L_i$ is the aspect ratio of transistor M_i.

If $\alpha_1 = \alpha_2$, and $\alpha_3 = \alpha_4$ then:

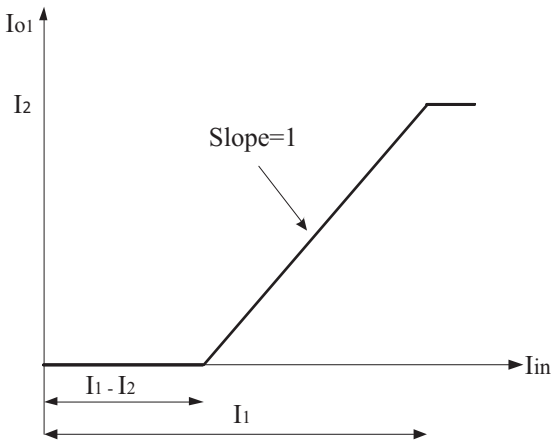
$$I_{o1} = I_2 - I_1 + I_{in}. \tag{2}$$

With reference to Fig. 5a, if $I_{in} > I_1$, then M1 and M2 will be OFF, current I_2 will be forced to go through M3 giving $I_{o1} = I_2$. If $I_{in} < I_1 - I_2$ then the output current will be forced to be negative, which is impossible. Thus, I_{o1} will be equal to zero. This is summarized in (3).

$$I_{o1} = \begin{cases} I_2 & \text{if } I_{in} \geq I_1, \\ 0 & \text{if } I_{in} \leq I_1 - I_2. \end{cases} \tag{3}$$

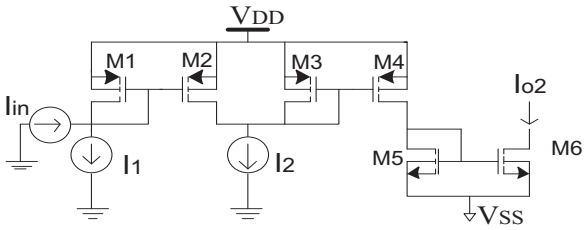


(a) Circuit diagram

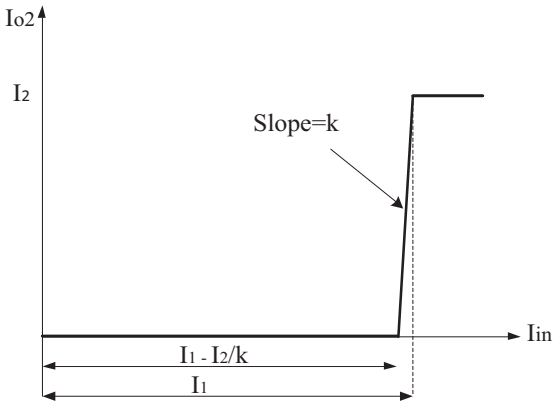


(b) Transfer curve

Fig. 5. Block 1 circuit diagram and transfer curve.



(a) Circuit diagram



(b)Transfer curve

Fig. 6. Block 2 circuit diagram and transfer curve.

A possible realization for block2 of Fig. 4, with an inverted output, is shown in Fig. 6(a). The input-output characteristic of the circuit of Fig. 6(a) is shown in Fig. 6(b).

$$I_{o2} = I_2 \frac{\alpha_4}{\alpha_3} - I_1 \frac{\alpha_2\alpha_4}{\alpha_1\alpha_3} + I_{in} \frac{\alpha_2\alpha_4}{\alpha_1\alpha_3}. \tag{4}$$

If $\alpha_3 = \alpha_4$ then:

$$I_{o2} = I_2 - I_1 \frac{\alpha_2}{\alpha_1} + I_{in} \frac{\alpha_2}{\alpha_1}, \tag{5}$$

$$I_{o2} = I_2 - k(I_1 - I_{in}) \tag{6}$$

where $k = \alpha_2 / \alpha_1$.

With reference to Fig. (6a), if $I_{in} \geq I_1$, then M1 and M2 will be OFF and the current I_2 will be forced through M3 giving:

$$I_{o2} = I_2.$$

Now, if $I_{in} = I_1 - I_2 / k$, (6) can be written as:

$$I_{o2} = I_2 - I_1 k + k\left(I_1 - \frac{I_2}{k}\right) = 0. \tag{7}$$

If $I_{in} < I_1 - \frac{I_2}{k} = \beta\left(I_1 - \frac{I_2}{k}\right)$, with $\beta < 1$, then

$$I_{o2} = I_2 - k\left(I_1 - \beta\left(I_1 - \frac{I_2}{k}\right)\right), \tag{8}$$

$$I_{o2} = (1-\beta)(I_2 - kI_1). \tag{9}$$

With $I_2 < I_1$ and $k > 1$, I_{o2} will be negative and this is impossible. Thus I_{o2} is forced to be equal to 0.

This can be summarized as follows:

$$I_{o2} = \begin{cases} I_2; & \text{if } I_{in} \geq I_1, \\ 0; & \text{if } I_{in} \leq I_1 - \frac{I_2}{k}. \end{cases} \tag{10}$$

The output current of Fig. 4 will be the sum of the two currents, that is

$$I_{out} = I_{o1} - I_{o2}. \tag{11}$$

Inspection of equations (3), (10) and (11) shows that the input-output characteristic of Fig. 4 can be obtained by proper selection of the biasing currents I_1 and I_2.

In the previous analysis it was assumed that $\alpha_1 = \alpha_2$, and $\alpha_3 = \alpha_4$. This resulted in a slope = 1 for the characteristic of Fig. 4. However, in general, using (1), the slope of the transfer characteristic for blocks 1 and 2 of Fig. 4 is given by:

$$S = \frac{\alpha_2\alpha_4}{\alpha_1\alpha_3}.$$

It is worth mentioning here that the slope S can be controlled by the aspect ratios of transistors M1-M4.

The complete circuit diagram of the proposed current mode folding amplifier with a folding factor of 4 is shown in Fig. 7 with all MOSFETs substrates connected to the respected sources.

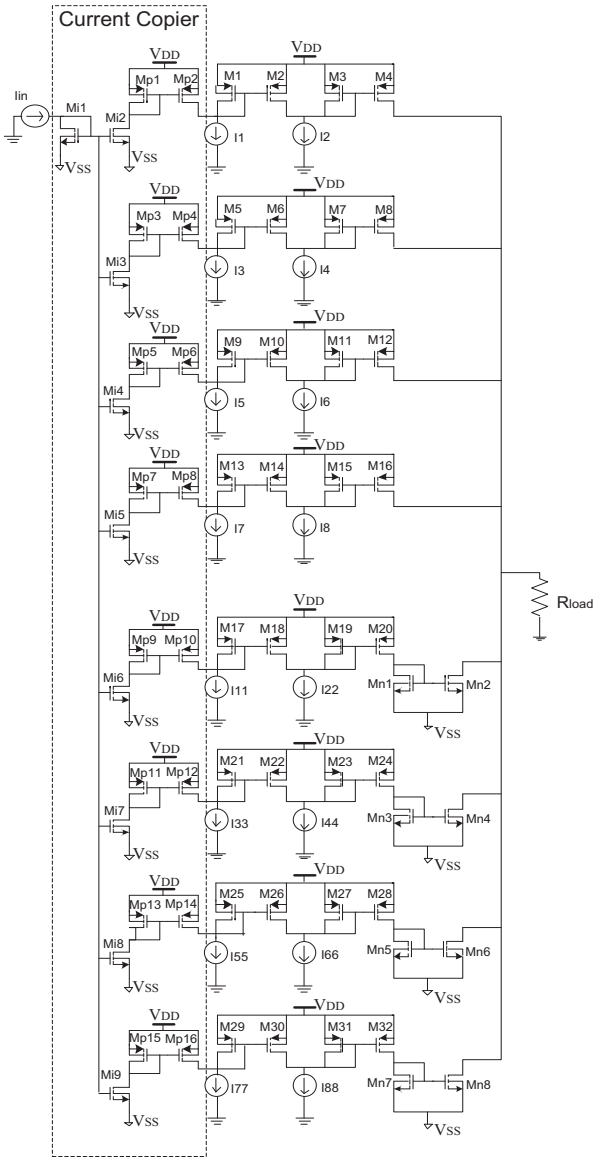


Fig. 7. Current-mode folding amplifier with a folding factor of 4.

4. Simulation Results and Discussion

The proposed circuit of Fig. 7 was simulated using Tanner simulation tools in 0.35 μm CMOS process technology with DC supply voltage VDD = − VSS = 1 V and bias currents as follows;

$$I_1 = I_{11} = 9\ \mu\text{A},$$

$$I_2 = I_{22} = I_4 = I_{44} = I_6 = I_{66} = I_8 = I_{88} = 9\ \mu\text{A},$$

$$I_7 = I_{77} = 4I_1,$$

$$I_5 = I_{55} = 3I_1,$$

$$\text{and } I_3 = I_{33} = 2I_1.$$

The output current was measured by forcing it through a grounded resistive load of 1 kΩ. All transistors aspect ratios are given in Tab. 1.

Transistor	Aspect ratio
M1,M2,M5,M6 M9,M10,M13,M14 M17,M21,M25,M29	2 μm /2 μm
M3,M4,M7,M8M11,M12,M15,M16,M19,M 20,M23,M24M27,M28,M31,M32	4 μm/ 2μm
M18,M22,M26,M30	50 μm/2 μm
Mi1-Mi9 &Mp1-Mp16	20 μm/4 μm
Mn1,Mn2,Mn3,Mn4Mn5,Mn6,Mn7,Mn8	2.4 μm/2 μm

Tab. 1. Transistors aspect ratios.

4.1 DC Simulation Results

The DC simulation results of the proposed folding amplifier are shown in Fig. 8. It appears from Fig. 8 that the simulated result is a saw-tooth-shape which confirms the functionality of the developed design.

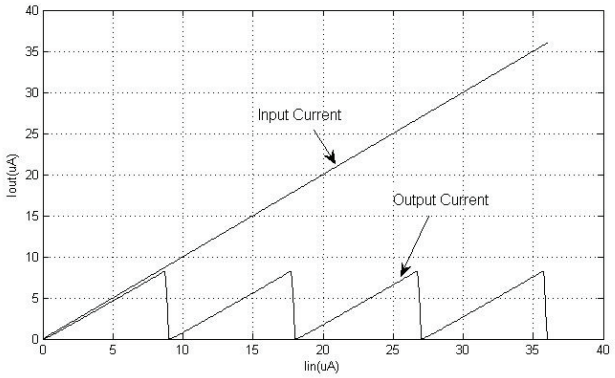


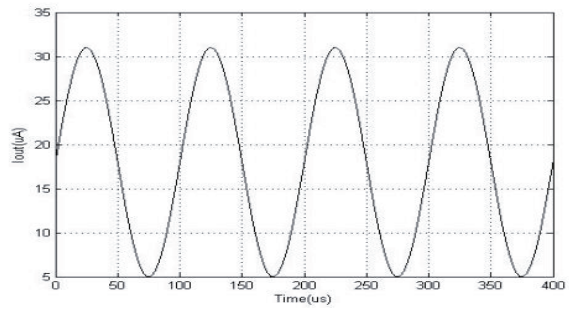
Fig. 8. Input and output characteristics of current-mode amplifier.

4.2 Transient Simulation Results

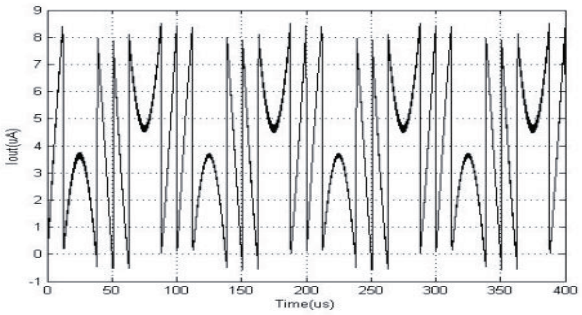
The proposed circuit was simulated for transient analysis. The input is a sine wave signal as shown in Fig. 9(a). It is evident from Fig. 9(b) that simulation result confirms the functionality of the circuit.

5. Mismatch Analysis

Since the design is based on current mirrors, the accuracy of the folding amplifier will be affected by the mirror performance. Consequently, it is important to study the effect of mismatch in device dimension that may result during fabrication process [10]. With reference to the core circuits in Fig. 5(a) and Fig. 6(a) assuming a mismatch in the threshold voltages between M1 and M2 such that α_p is the average of α_{p1} and α_{p2}, and $\Delta\alpha_p$ is the mismatch, where α_{p1} and α_{p2} are the aspect ratios of transistors M1 and M2 forming the mirror respectively and assuming all other parameters are matched, the mirrored current in M2 is given by:



(a) Input signal



(b) Folded output signal

Fig. 9. Transient response of current-mode folding amplifier.

$$I_{M2} = I_{M2}\left(1+\frac{\Delta\alpha_p}{\alpha_p}\right). \tag{12}$$

Similarly, If α_n is the average of α_{p3} and α_{p4}, and $\Delta\alpha_n$ is the mismatch, where α_{p3} and α_{p4} are the aspect ratios of transistors M3 and M4, the mirrored current in M4 is given by:

$$I_{M4} = I_{M3}\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right). \tag{13}$$

It is obvious from (12) that reducing the effect of mismatch can be achieved by increasing the transistor aspect ratio α_p. Using (11), (1) can be written as:

$$I_{o1} = I_2\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right) - I_1\left(1+\frac{\Delta\alpha_p}{\alpha_p}\right)\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right) + I_{in}\left(1+\frac{\Delta\alpha_p}{\alpha_p}\right)\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right). \tag{14}$$

Similarly, the current I_{o2} can be written as

$$I_{o2} = I_2\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right) - I_1\left(1+\frac{\Delta\alpha_p}{\alpha_p}\right)\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right) + I_{in}\left(1+\frac{\Delta\alpha_p}{\alpha_p}\right)\left(1+\frac{\Delta\alpha_n}{\alpha_n}\right). \tag{15}$$

Equations (14) and (15) can be written as:

$$I_{o1} = I_2K_1 - I_1K_1K_2 + I_{in}K_1K_2, \tag{16}$$

$$I_{o2} = I_2K_1 - I_1K_1K_2 + I_{in}K_1K_2. \tag{17}$$

It is clear form (16) and (17) the currents I_1 and I_{in} will have the same coefficient, which means that (3) and (10) are valid even if there is a mismatch in aspects ratio. However there will be a small gain error which can be reduced by reducing K_1.

Monte Carlo analysis was carried out with the variance set to 0.02. Since the statistical significance of 30 iterations is quite high, a 30-iteration Monte Carlo analysis was performed. The results are shown in Fig. 10 for 30 iterations. It is clearly shown that the maximum variation is 0.6 μA which is acceptable in terms of a 5-bit ADC where the LSB is around 1 μA.

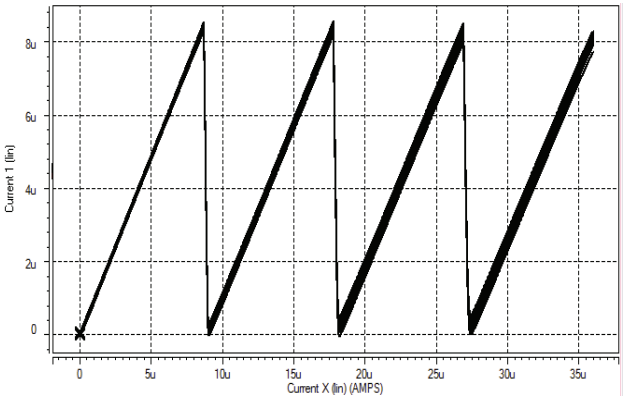


Fig. 10. Effect of process variations (W/L) on the DC characteristic.

Simulation for temperature effects was carried out. The temperature was swept from −25 °C to 75 °C in steps of 50 °C. The simulation result shown in Fig. 11 confirms that the circuit is insensitive to temperature variations.

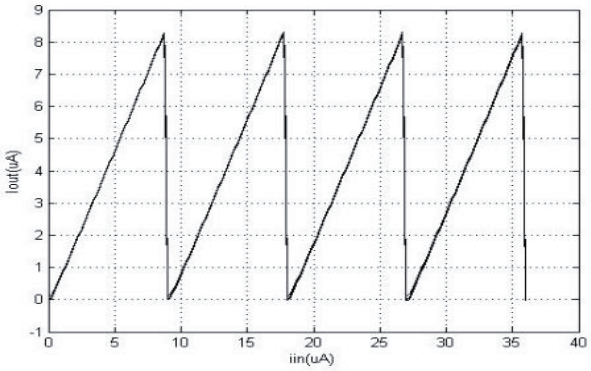


Fig. 11. Effect of temperature variations on DC characteristic.

Simulation for effect of power supply variations was also carried out. The supply voltage was varied between 0.9 V and 1.1 V in steps of 0.1 V. Simulation results shown in Fig. 12 indicate that the folded signal shape is still saw-tooth type.

6. Noise Analysis

Noise analysis was carried out. The frequency is swept up to 1 GHz. Simulation result shown in Fig. 13 indicates the noise is 1 nA at 0.5 GHz. The noise level is acceptable for a frequency up to 0.5 GHz since the circuit current range is few μA.

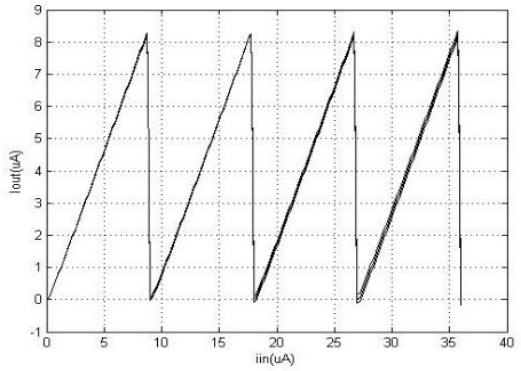


Fig. 12. Effect of power supply variations on DC characteristic.

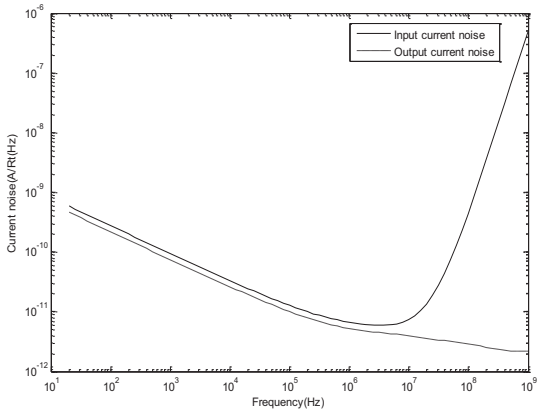


Fig. 13. Noise analysis.

7. Conclusion

A new CMOS current-mode folding amplifier was proposed. Simulation results confirm that the proposed circuit produces a saw-tooth input-output characteristic which will improve the accuracy of current-mode folding ADC. Also, simulation results indicate that the circuit is almost insensitive to process, temperature and power supply variations. The proposed circuit's total power consumption is 519 μW. We believe that this circuit will be an important building block in current-mode folding ADC design.

Acknowledgements

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